Abstract

A method of manufacturing a layer sequence and a method of manufacturing an integrated circuit

A method of manufacturing a layer sequence having a first and a second laterally confined structure comprises the steps of providing a first layer on a first surface portion of a substrate, which first layer is doped with dopant of a first type of conductivity, providing a second layer on a second surface portion of the substrate, which second layer is free of dopant of the first type of conductivity, forming a third layer on the first layer, which third layer is free of dopant of the first type of conductivity, and forming a fourth layer on the second layer, which forth layer is doped with dopant of the first type of conductivity. The first layer and the third layer are etched, thereby patterning the first and third layer to form the first laterally confined structure. The second layer and the forth layer are etched, thereby patterning the second and fourth layer to form the second laterally confined structure.